IDEC Chip Design Contest

A WR-3.4 Band Phase Shifter With Active SPDT Switches

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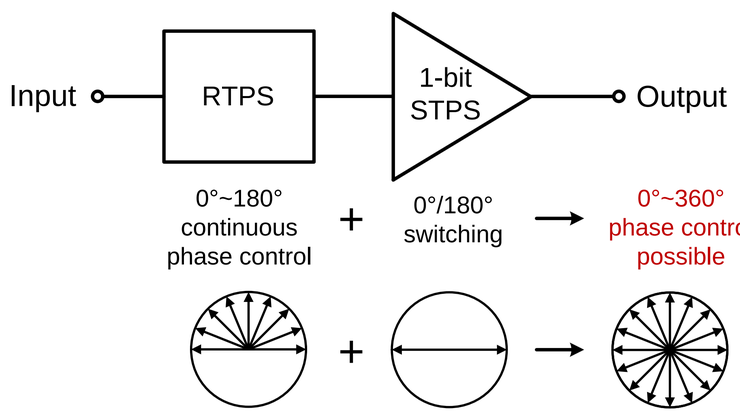
Introduction

- In the subterahertz band, a phased array is widely adopted as one of the solutions to overcome the high channel loss and tight link budget.
- A phase shifter is a core circuit block that controls the phase of each channel of the phased-array system.
- WR-3.4 360° phase shifter with active SPDT switches fabricated in 250-nm InP HBT is presented.

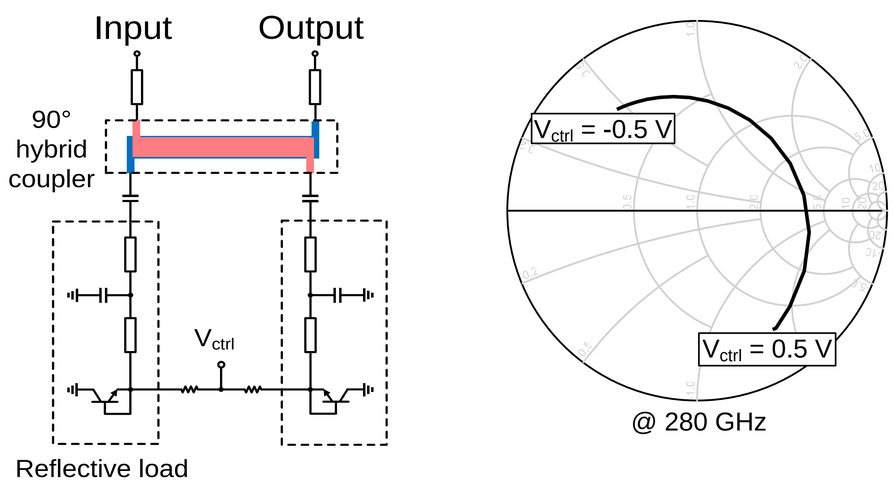
Phase Shifter Design

Block diagram of the proposed phase shifter



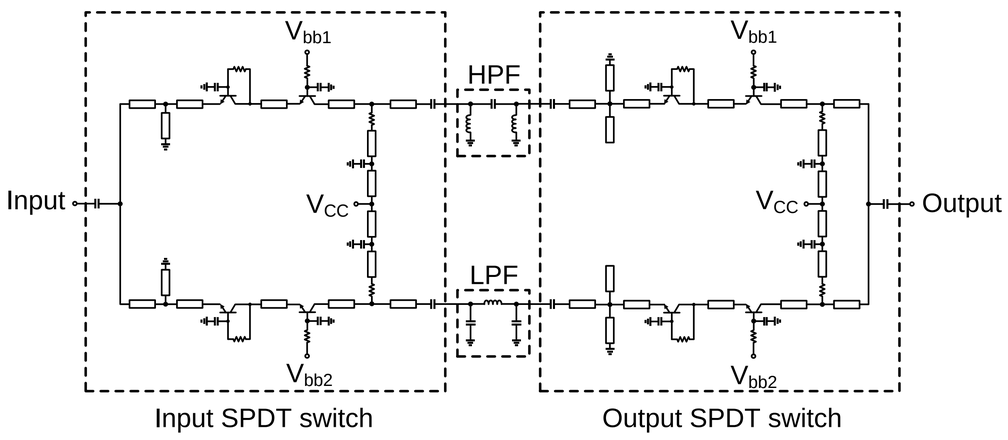
- By combining a 180° reflection-type phase shifter (RTPS) and 1-bit switching-type phase shifter (STPS), the proposed phase shifter achieves a continuous full 360° phase shift range.
- In particular, the single-pole double-throw (SPDT) switches constituting the 1-bit STPS adopts active topology to compensate for insertion loss of the passive RTPS.

180° RTPS



- The RTPS consists of 90° hybrid coupler and the C-L-C reflective load to achieve 180° phase shift range.
- The 90° hybrid coupler is implemented using a broadside-coupled line structure for compact chip size.
- The reference impedance of the reflective load is set to 30-Ω, resulting in low loss variation over a wide frequency range.

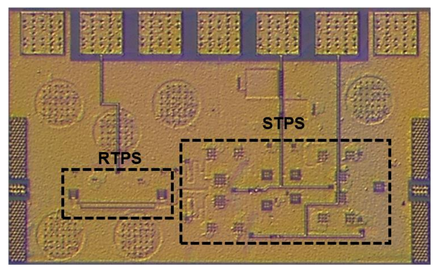
1-bit STPS

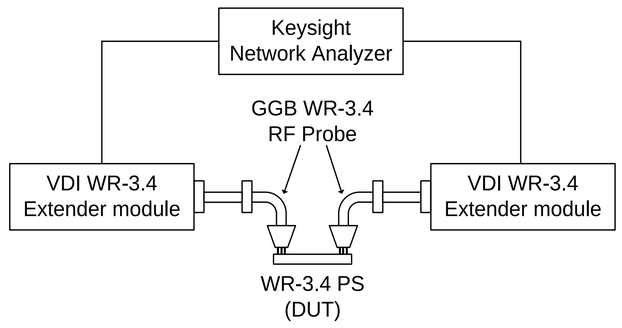


- The active SPDT switches are implemented in a 2-stage common-base topology for sufficient gain and isolation.
- The transistor of first CB stage is self-biased through a large resistor between collector and base, and by applying a base voltage to the second CB stage, the direction in which the signal passes is determined.
- The LPF and HPF are adopted to achieve 1-bit 180° phase delay.

Measurement Results

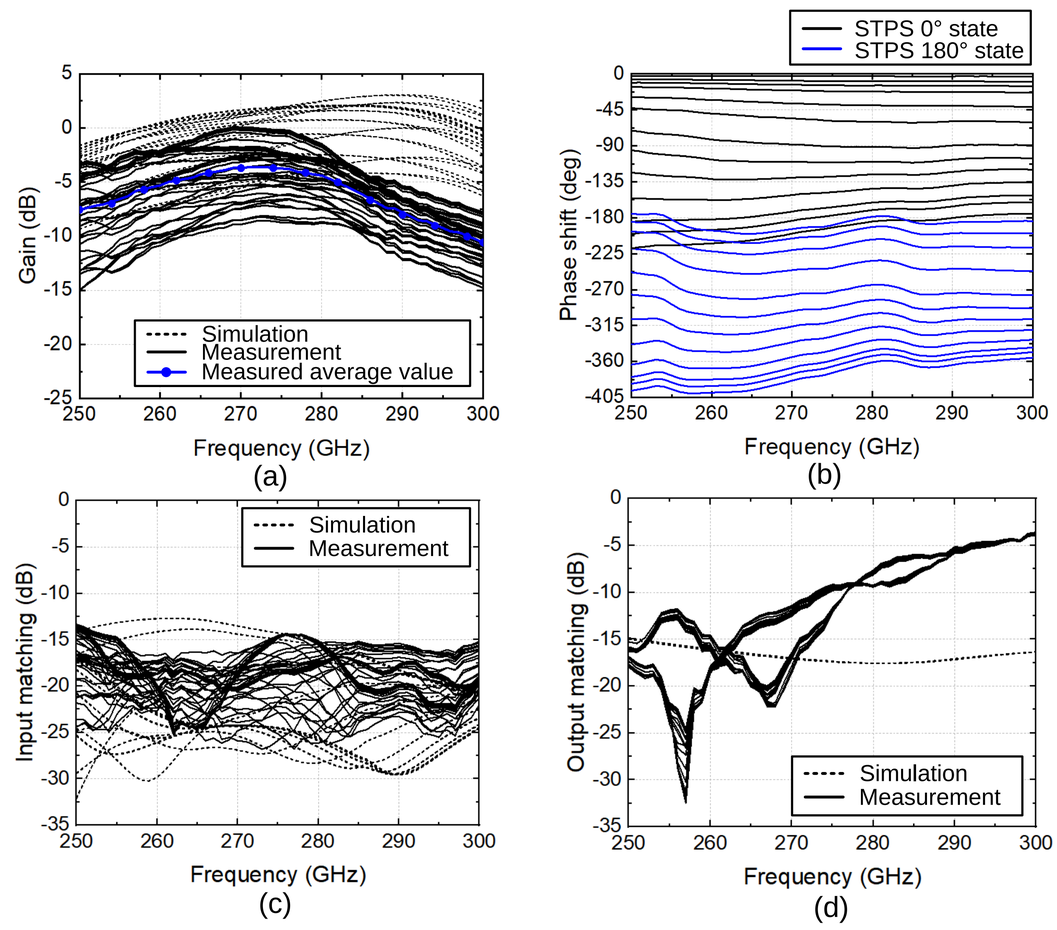
Chip micrograph and S-parameter measurement setup





- 250-nm InP DHBT technology
- Chip size : 0.71 × 0.43 mm^2
- The S-parameters were measured with a Keysight N5227A network analyzer and VDI WR-3.4 extension modules using 60-μm pitch ground-signal-ground (GSG) on-wafer probes.

Measurement results



- Peak average gain = -3.6 dB @ 272 GHz
- 3-dB BW = 32 GHz (255 – 286 GHz)
- Phase shift range > 360°
- Input return loss < -10 dB @ 250–300 GHz
- Output return loss < -10 dB @ 250–273 GHz
- P_{DC} = 33 mW

Conclusion

- WR-3.4 band phase shifter is implemented in 250-nm InP technology
- RTPS and active STPS are combined for 360° phase shifting range and comparable insertion loss

The chip was fabricated using the Teledyne 250-nm InP DHBT process supported by the IC Design Education Center(IDEC), Korea.